

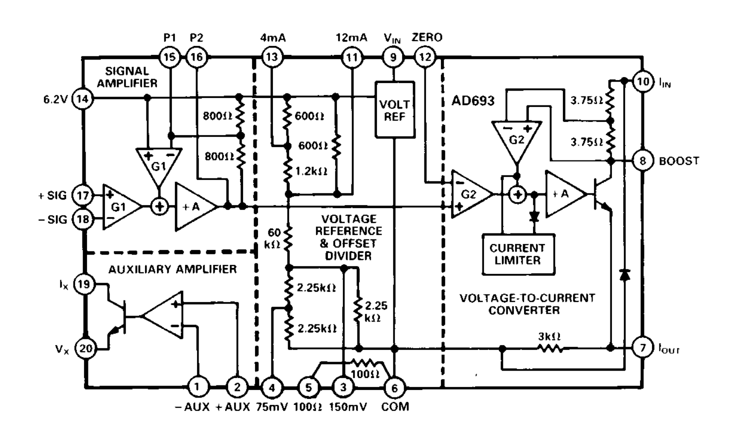
Loop-Powered 4–20 mA Sensor Transmitter

AD693

FEATURES

Instrumentation Amplifier Front End
Loop-Powered Operation
Precalibrated 30 mV or 60 mV Input Spans
Independently Adjustable Output Span and Zero
Precalibrated Output Spans: 4–20 mA Unipolar
0–20 mA Unipolar
12 ± 8 mA Bipolar
Precalibrated 100 Ω RTD Interface
6.2 V Reference with Up to 3.5 mA of Current Available
Uncommitted Auxiliary Amp for Extra Flexibility
Optional External Pass Transistor to Reduce Self-Heating Errors

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD693 is a monolithic signal conditioning circuit which accepts low-level inputs from a variety of transducers to control a standard 4–20 mA, two-wire current loop. An on-chip voltage reference and auxiliary amplifier are provided for transducer excitation; up to 3.5 mA of excitation current is available when the device is operated in the loop-powered mode. Alternatively, the device may be locally powered for three-wire applications when 0–20 mA operation is desired.

Precalibrated 30 mV and 60 mV input spans may be set by simple pin strapping. Other spans from 1 mV to 100 mV may be realized with the addition of external resistors. The auxiliary amplifier may be used in combination with on-chip voltages to provide six precalibrated ranges for 100 Ω RTDs. Output span and zero are also determined by pin strapping to obtain the standard ranges: 4–20mA, 12 ± 8 mA and 0–20 mA.

Active laser trimming of the AD693's thin-film resistors result in high levels of accuracy without the need for additional adjustments and calibration. Total unadjusted error is tested on every device to be less than 0.5% of full scale at +25°C, and less than 0.75% over the industrial temperature range. Residual nonlinearity is under 0.05%. The AD693 also allows for the use of an external pass transistor to further reduce errors caused by self-heating.

For transmission of low-level signals from RTDs, bridges and pressure transducers, the AD693 offers a cost-effective signal conditioning solution. It is recommended as a replacement for discrete designs in a variety of applications in process control, factory automation and system monitoring.

The AD693 is packaged in a 20-pin ceramic side-brazed DIP, 20-pin Cerdip, and 20-pin LCCC and is specified over the –40°C to +85°C industrial temperature range.

PRODUCT HIGHLIGHTS

1. The AD693 is a complete monolithic low-level voltage-to-current loop signal conditioner.
2. Precalibrated output zero and span options include 4–20 mA, 0–20 mA, and 12 ± 8 mA in two- and three-wire configurations.
3. Simple resistor programming adds a continuum of ranges to the basic 30 mV and 60 mV input spans.
4. The common-mode range of the signal amplifier input extends from ground to near the device's operating voltage.
5. Provision for transducer excitation includes a 6.2 V reference output and an auxiliary amplifier which may be configured for voltage or current output and signal amplification.
6. The circuit configuration permits simple linearization of bridge, RTD, and other transducer signals.
7. A monitored output is provided to drive an external pass transistor. This feature off-loads power dissipation to extend the temperature range of operation, enhance reliability, and minimize self-heating errors.
8. Laser-wafer trimming results in low unadjusted errors and affords precalibrated input and output spans.
9. Zero and span are independently adjustable and noninteractive to accommodate transducers or user defined ranges.
10. Six precalibrated temperature ranges are available with a 100 Ω RTD via pin strapping.

REV. A

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AD693–SPECIFICATIONS

(@ +25°C and V_S = +24 V. Input Span = 30 mV or 60 mV. Output Span = 4–20 mA, R_L = 250 Ω, V_{CM} = 3.1 V, with external pass transistor unless otherwise noted.)

Model	Conditions	AD693AD/AQ/AE Min	Typ	Max	Units
LOOP-POWERED OPERATION					
TOTAL UNADJUSTED ERROR[1, 2]			±0.25	**±0.5**	% Full Scale
T_{MIN} to T_{MAX}			±0.4	**±0.75**	% Full Scale
100 Ω RTD CALIBRATION ERROR[3]	(See Figure 17)		±0.5	±2.0	°C
LOOP POWERED OPERATION[2]					
Zero Current Error[4]	Zero = 4 mA		±25	**±80**	µA
	Zero = 12 mA		±40	**±120**	µA
	Zero = 0 mA[5]	+7	+35	**+100**	µA
vs. Temp.	Zero = 4 mA		±0.5	±1.5	µA/°C
Power Supply Rejection (RTI)	12 V ≤ V_{OP} ≤ 36V[6]		±3.0	**±5.6**	µV/V
	0 V ≤ V_{CM} ≤ 6.2 V				
Common-Mode Input Range	(See Figure 3)	0		+V_{OP} – 4 V[6]	V
Common-Mode Rejection (RTI)	0 V ≤ V_{CM} ≤ 6.2 V		±10	**±30**	µV/V
Input Bias Current[7]			+5	**+20**	nA
T_{MIN} to T_{MAX}			+7	**+25**	nA
Input Offset Current[7]	V_{SIG} = 0		±0.5	**±3.0**	nA
Transconductance					
Nominal	30 mV Input Span		0.5333		A/V
	60 mV Input Span		0.2666		A/V
Unadjusted Error			±0.05	**±0.2**	%
vs. Common-Mode	0 V ≤ V_{CM} ≤ 6.2 V				
	30 mV Input Span		±0.03	±0.04	%/V
	60 mV Input Span		±0.05	±0.06	%/V
Error vs. Temp.			±20	±50	ppm/°C
Nonlinearity[8]	30 mV Input Span		±0.01	**±0.05**	% of Span
	60 mV Input Span		±0.02	**±0.07**	% of Span
OPERATIONAL VOLTAGE RANGE					
Operational Voltage, V_{OP}[6]		**+12**		**+36**	V
Quiescent Current	Into Pin 9		+500	**+700**	µA
OUTPUT CURRENT LIMIT		**+21**	+25	**+32**	mA
COMPONENTS OF ERROR					
SIGNAL AMPLIFIER[9]					
Input Voltage Offset			±40	**±200**	µV
vs. Temp			±1.0	±2.5	µV/°C
Power Supply Rejection	12 V ≤ V_{OP} ≤ 36 V[6]		±3.0	**±5.6**	µV/V
	0 V ≤ V_{CM} ≤ 6.2 V				
V/I CONVERTER[9, 10]					
Zero Current Error	Output Span = 4–20 mA		±30	±80	µA
Power Supply Rejection	12 V ≤ V_{OP} ≤ 36 V[6]		±1.0	±3.0	µA/V
Transconductance					
Nominal			0.2666		A/V
Unadjusted Error			±0.05	±0.2	%
6.200 V REFERENCE[9, 12]					
Output Voltage Tolerance			±3	**±12**	mV
vs. Temp.			±20	±50	ppm/°C
Line Regulation	12 V ≤ V_{OP} ≤ 36 V[6]		±200	**±300**	µV/V
Load Regulation[11]	0 mA ≤ I_{REF} ≤ 3 mA		±0.3	**±0.75**	mV/mA
Output Current[13]	Loop Powered, (Figure 10)	**+3.0**	+3.5		mA
	3-Wire Mode, (Figure 15)		+5.0		mA

Model	Conditions	AD693AD Min	Typ	Max	Units
AUXILIARY AMPLIFIER					
Common-Mode Range		0		$+V_{OP} - 4$ V[6]	V
Input Offset Voltage			±50	±200	μV
Input Bias Current			+5	+20	nA
Input Offset Current			+0.5	±3.0	nA
Common-Mode Rejection			90		dB
Power Supply Rejection			105		dB
Output Current Range	Pin I_X OUT	+0.01		+5	mA
Output Current Error	Pin V_X – Pin I_X		±0.005		%
TEMPERATURE RANGE					
Case Operating[14]	T_{MIN} to T_{MAX}	–40		+85	°C
Storage		–65		+150	°C

NOTES
[1] Total error can be significantly reduced (typically less than 0.1%) by trimming the zero current. The remaining unadjusted error sources are transconductance and nonlinearity.
[2] The AD693 is tested as a loop powered device with the signal amp, V/I converter, voltage reference, and application voltages operating together. Specifications are valid for preset spans and spans between 30 mV and 60 mV.
[3] Error from ideal output assuming a perfect 100 Ω RTD at 0 and +100°C.
[4] Refer to the Error Analysis to calculate zero current error for input spans less than 30 mV.
[5] By forcing the differential signal amplifier input sufficiently negative the 7 μA zero current can always be achieved.
[6] The operational voltage (V_{OP}) is the voltage directly across the AD693 (Pin 10 to 6 in two-wire mode, Pin 9 to 6 in local power mode). For example, $V_{OP} = V_S - (I_{LOOP} \times R_L)$ in two-wire mode (refer to Figure 10).
[7] Bias currents are not symmetrical with input signal level and flow out of the input pins. The input bias current of the inverting input increases with input signal voltage, see Figure 2.
[8] Nonlinearity is defined as the deviation of the output from a straight line connecting the endpoints as the input is swept over a 30 mV and 60 mV input span.
[9] Specifications for the individual functional blocks are components of error that contribute to, and that are included in, the Loop Powered Operation specifications.
[10] Includes error contributions of V/I converter and Application Voltages.
[11] Changes in the reference output voltage due to load will affect the Zero Current. A 1% change in the voltage reference output will result in an error of 1% in the value of the Zero Current.
[12] If not used for external excitation, the reference should be loaded by approximately 1 mA (6.2 kΩ to common).
[13] In the loop powered mode up to 5 mA can be drawn from the reference, however, the lower limit of the output span will be increased accordingly. 3.5 mA is the maximum current the reference can source while still maintaining a 4 mA zero.
[14] The AD693 is tested with a pass transistor so $T_A \cong T_C$.
Specifications subject to change without notice.
Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

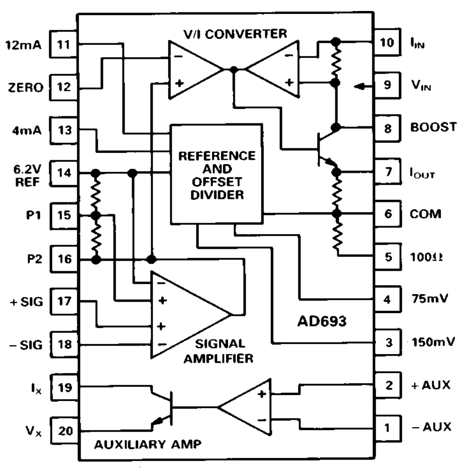
ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . +36 V
Reverse Loop Current . . . . 200 mA
Signal Amp Input Range . . . . –0.3 V to V_{OP}
Reference Short Circuit to Common . . . . Indefinite
Auxiliary Amp Input Voltage Range . . . . 0.3 V to V_{OP}
Auxiliary Amp Current Output . . . . 10 mA
Storage Temperature . . . . –65°C to +150°C
Lead Temperature, 10 sec Soldering . . . . +300°C
Max Junction Temperature . . . . +150°C

ORDERING GUIDE

Model	Package Description	Package Option
AD693AD	Ceramic Side-Brazed DIP	D-20
AD693AQ	Cerdip	Q-20
AD693AE	Leadless Ceramic Chip Carrier (LCCC)	E-20A

AD693 PIN CONFIGURATION (AD, AQ, AE Packages)



Functional Diagram

AD693–Typical Characteristics

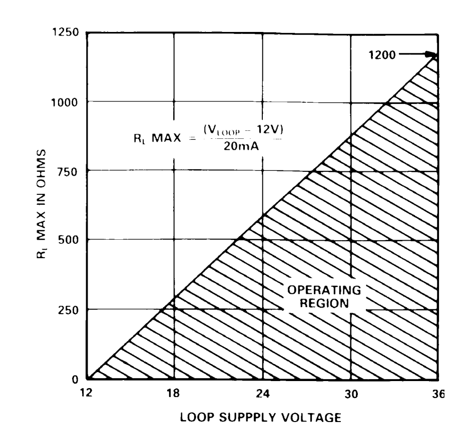


Figure 1. Maximum Load Resistance vs. Power Supply

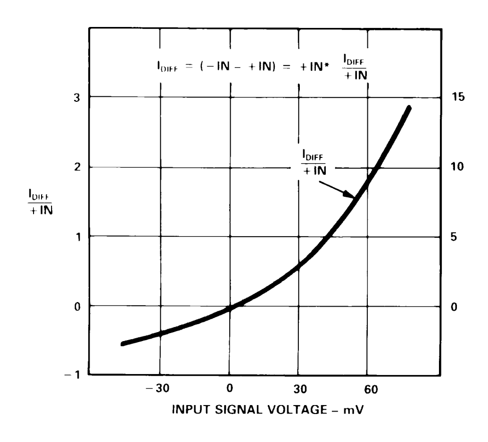


Figure 2. Differential Input Current vs. Input Signal Voltage Normalized to +IN

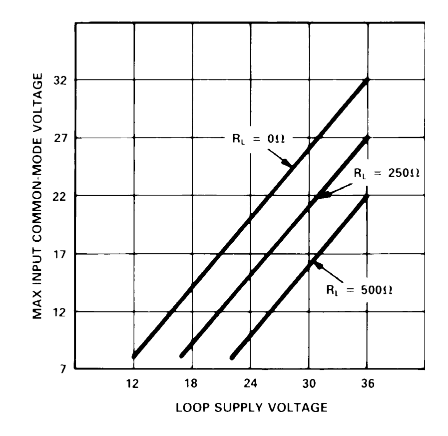


Figure 3. Maximum Common-Mode Voltage vs. Supply

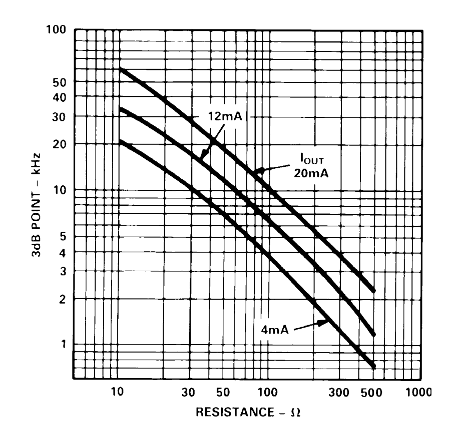


Figure 4. Bandwidth vs. Series Load Resistance

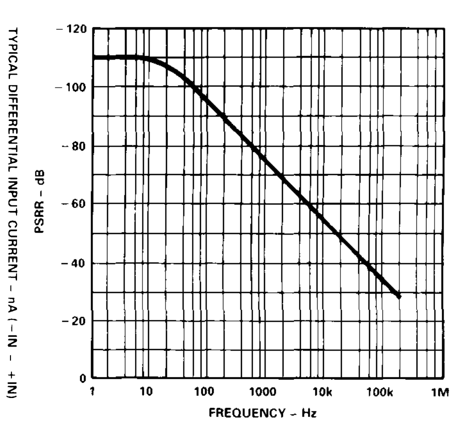


Figure 5. Signal Amplifier PSRR vs. Frequency

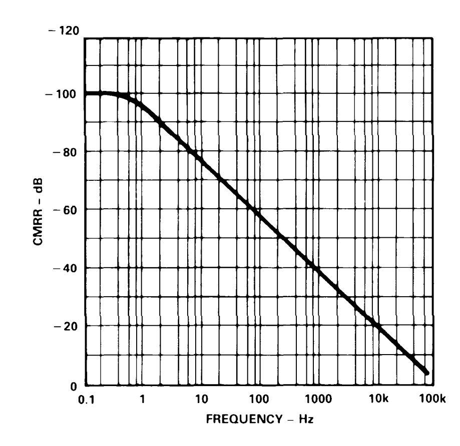


Figure 6. CMRR (RTI) vs. Frequency

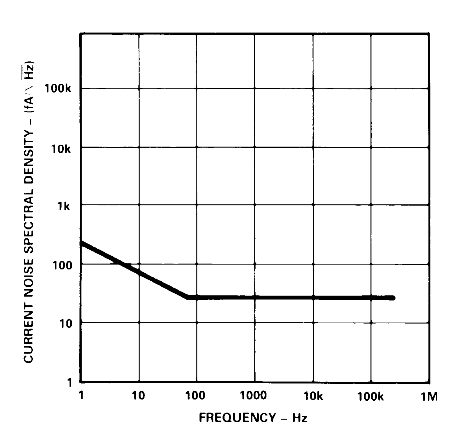


Figure 7. Input Current Noise vs. Frequency

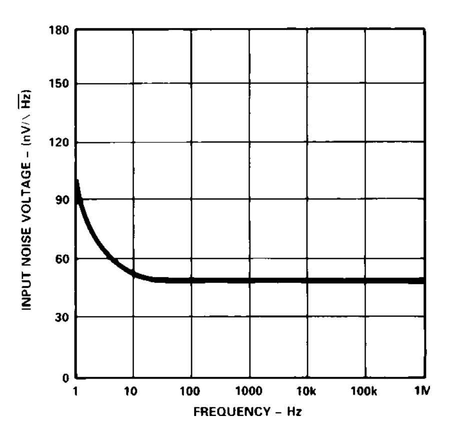


Figure 8. Input Voltage Noise vs. Frequency

FUNCTIONAL DESCRIPTION

The operation of the AD693 can be understood by dividing the circuit into three functional parts (see Figure 9). First, an instrumentation amplifier front-end buffers and scales the low-level input signal. This amplifier drives the second section, a V/I converter, which provides the 4-to-20mA loop current. The third section, a voltage reference and resistance divider, provides application voltages for setting the various "live zero" currents. In addition to these three main sections, there is an on-chip auxiliary amplifier which can be used for transducer excitation.

VOLTAGE-TO-CURRENT (V/I) CONVERTER

The output NPN transistor for the V/I section sinks loop current when driven on by a high gain amplifier at its base. The input for this amplifier is derived from the difference in the outputs of the matched preamplifiers having gains, G2. This difference is caused to be small by the large gain, +A, and the negative feedback through the NPN transistor and the loop current sampling resistor between I_{IN} and Boost. The signal across this resistor is compared to the input of the left preamp and servos the loop current until both signals are equal. Accurate voltage-to-current transformation is thereby assured. The preamplifiers employ a special design which allows the active feedback amplifier to operate from the most positive point in the circuit, $I_{IN.}$

The V/I stage is designed to have a nominal transconductance of 0.2666 A/V. Thus, a 75 mV signal applied to the inputs of the V/I (Pin 16, noninverting; Pin 12, inverting) results in a full-scale output current of 20 mA.

The current limiter operates as follows: the output of the feedback preamp is an accurate indication of the loop current. This output is compared to an internal setpoint which backs off the drive to the NPN transistor when the loop current approaches 25 mA. As a result, the loop and the AD693 are protected from the consequences of voltage overdrive at the V/I input.

VOLTAGE REFERENCE AND DIVIDER

A stabilized bandgap voltage reference and laser-trimmed resistor divider provide for both transducer excitation as well as precalibrated offsets for the V/I converter. When not used for external excitation, the reference should be loaded by approximately 1 mA (6.2 kΩ to common).

The 4 mA and 12 mA taps on the resistor divider correspond to –15 mV and –45 mV, respectively, and result in a live zero of 4 mA or 12 mA of loop current when connected to the V/I converter's inverting input (Pin 12). Arranging the zero offset in this way makes the zero signal output current independent of input span. When the input to the signal amp is zero, the noninverting input of the V/I is at 6.2 V.

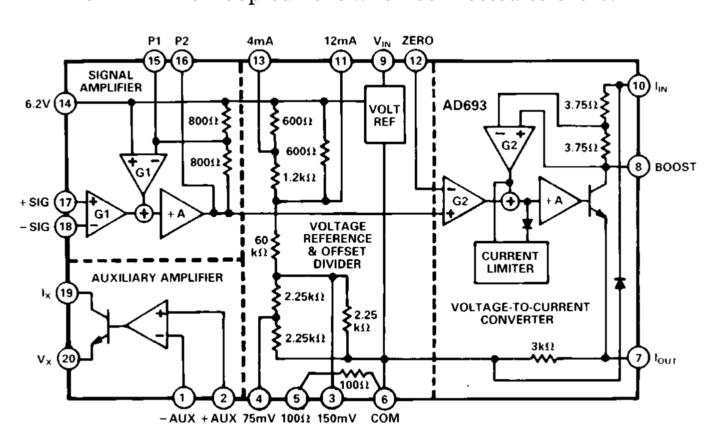


Figure 9. Functional Flock Diagram

Since the standard offsets are laser trimmed at the factory, adjustment is seldom necessary except to accommodate the zero offset of the actual source. (See "Adjusting Zero.")

SIGNAL AMPLIFIER

The Signal Amplifier is an instrumentation amplifier used to buffer and scale the input to match the desired span. Inputs applied to the Signal Amplifier (at Pins 17 and 18) are amplified and referred to the 6.2 V reference output in much the same way as the level translation occurs in the V/I converter. Signals from the two preamplifiers are subtracted, the difference is amplified, and the result is fed back to the upper preamp to minimize the difference. Since the two preamps are identical, this minimum will occur when the voltage at the upper preamp just matches the differential input applied to the Signal Amplifier at the left.

Since the signal which is applied to the V/I is attenuated across the two 800 Ω resistors before driving the upper preamp, it will necessarily be an amplified version of the signal applied between Pins 17 and 18. By changing this attenuation, you can control the span referred to the Signal Amplifier. To illustrate: a 75 mV signal applied to the V/I results in a 20 mA loop current. Nominally, 15 mV is applied to offset the zero to 4 mA leaving a 60 mV range to correspond to the span. And, since the nominal attenuation of the resistors connected to Pins 16, 15 and 14 is 2.00, a 30 mV input signal will be doubled to result in 20 mA of loop current. Shorting Pins 15 and 16 results in unity gain and permits a 60 mV input span. Other choices of span may be implemented with user supplied resistors to modify the attenuation. (See section "Adjusting Input Span.")

The Signal Amplifier is specially designed to accommodate a large common-mode range. Common-mode signals anywhere up to and beyond the 6.2 V reference are easily handled as long as V_{IN} is sufficiently positive. The Signal Amplifier is biased with respect to V_{IN} and requires about 3.5 volts of headroom. The extended range will be useful when measuring sensors driven, for example, by the auxiliary amplifier which may go above the 6.2 V potential. In addition, the PNP input stage will continue to operate normally with common-mode voltages of several hundred mV, negative, with respect to common. This feature accommodates self-generating sensors, such as thermocouples, which may produce small negative normal-mode signals as well as common-mode noise on "grounded" signal sources.

AUXILIARY AMPLIFIER

The Auxiliary Amplifier is included in the AD693 as a signal conditioning aid. It can be used as an op amp in noninverting applications and has special provisions to provide a controlled current output. Designed with a differential input stage and an unbiased Class A output stage, the amplifier can be resistively loaded to common with the self-contained 100 Ω resistor or with a user supplied resistor.

As a functional element, the Auxiliary Amplifier can be used in dynamic bridges and arrangements such as the RTD signal conditioner shown in Figure 17. It can be used to buffer, amplify and combine other signals with the main Signal Amplifier. The Auxiliary Amplifier can also provide other voltages for excitation

if the 6.2 V of the reference is unsuitable. Configured as a simple follower, it can be driven from a user supplied voltage divider or the precalibrated outputs of the AD693 divider (Pins 3 and 4) to provide a stiff voltage output at less than the 6.2 level, or by incorporating a voltage divider as feedback around the amplifier, one can gain-up the reference to levels higher than 6.2 V. If large positive outputs are desired, I_X, the Auxiliary Amplifier output current supply, should be strapped to either V_{IN} or Boost. Like the Signal Amplifier, the Auxiliary requires about 3.5 V of headroom with respect to V_{IN} at its input and about 2 V of difference between I_X and the voltage to which V_X is required to swing.

The output stage of the Auxiliary Amplifier is actually a high gain Darlington transistor where I_X is the collector and V_X is the emitter. Thus, the Auxiliary Amplifier can be used as a V/I converter when configured as a follower and resistively loaded. I_X functions as a high-impedance current source whose current is equal to the voltage at V_X divided by the load resistance. For example, using the onboard 100 Ω resistor and the 75 mV or 150 mV application voltages, either a 750 µA or 1.5 mA current source can be set up for transducer excitation.

The I_X terminal has voltage compliance within 2 V of V_X. If the Auxiliary Amplifier is not to be used, then Pin 2, the noninverting input, should be grounded.

REVERSE VOLTAGE PROTECTION FEATURE

In the event of a reverse voltage being applied to the AD693 through a current-limited loop (limited to 200 mA), an internal shunt diode protects the device from damage. This protection mode avoids the compliance voltage penalty which results from a series diode that must be added if reversal protection is required in high-current loops.

Applying the AD693

CONNECTIONS FOR BASIC OPERATION

Figure 10 shows the minimal connections for basic operation: 0–30 mV input span, 4–20 mA output span in the two-wire, loop-powered mode. If not used for external excitation, the 6.2 V reference should be loaded by approximately 1 mA (6.2 kΩ to common).

USING AN EXTERNAL PASS TRANSISTOR

The emitter of the NPN output section, I_{OUT}, of the AD693 is usually connected to common and the negative loop connection (Pins 7 to 6). Provision has been made to reconnect I_{OUT} to the base of a user supplied NPN transistor as shown in Figure 11. This permits the majority of the power dissipation to be moved off chip to enhance performance, improve reliability, and extend the operating temperature range. An internal hold-down resistor of about 3k is connected across the base emitter of the external transistor.

The external pass transistor selected should have a BV_{CEO} greater than the intended supply voltage with a sufficient power rating for continuous operation with 25 mA current at the supply voltage. Ft should be in the 10 MHz to 100 MHz range and β should be greater than 10 at a 20 mA emitter current. Some transistors that meet this criteria are the 2N1711 and 2N2219A. Heat sinking the external pass transistor is suggested.

The pass transistor option may also be employed for other applications as well. For example, I_{OUT} can be used to drive an LED connected to Common, thus providing a local monitor of loop fault conditions without reducing the minimum compliance voltage.

ADJUSTING ZERO

In general, the desired zero offset value is obtained by connecting an appropriate tap of the precision reference/voltage divider network to the inverting terminal of the V/I converter. As shown in Figure 9, precalibrated taps at Pins 14, 13 and 11 result in zero offsets of 0 mA, 4 mA and 12 mA, respectively, when connected to Pin 12. The voltages which set the 4 mA and 12 mA zero operating points are 15 mV and 45 mV negative with respect to 6.2 V, and they each have a nominal source resistance of 450 Ω. While these voltages are laser trimmed to high accuracy, they may require some adjustment to accommodate variability between sensors or to provide additional ranges. You can adjust zero by pulling up or down on the selected zero tap, or by making a separate voltage divider to drive the zero pin.

The arrangement of Figure 12 will give an approximately linear adjustment of the precalibrated options with fixed limits. To find the proper resistor values, first select I_A, the desired range

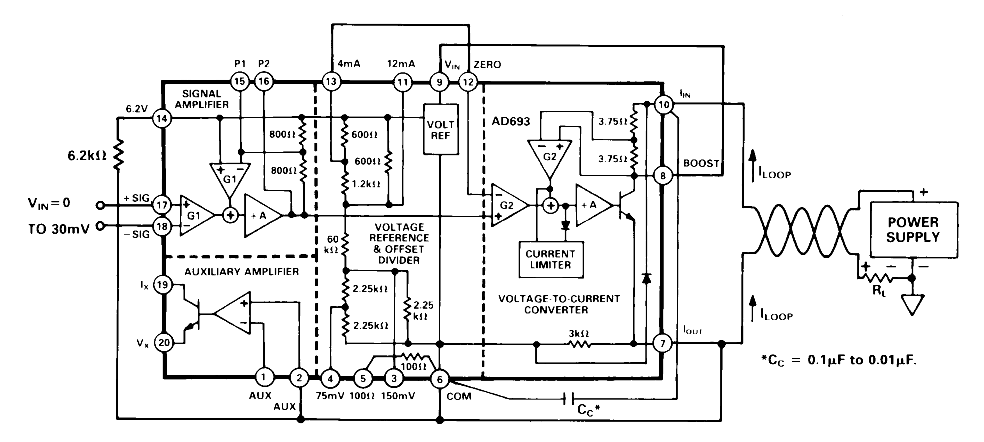


Figure 10. Minimal Connection for 0–30 mV Unipolar Input, 4–20 mA Output

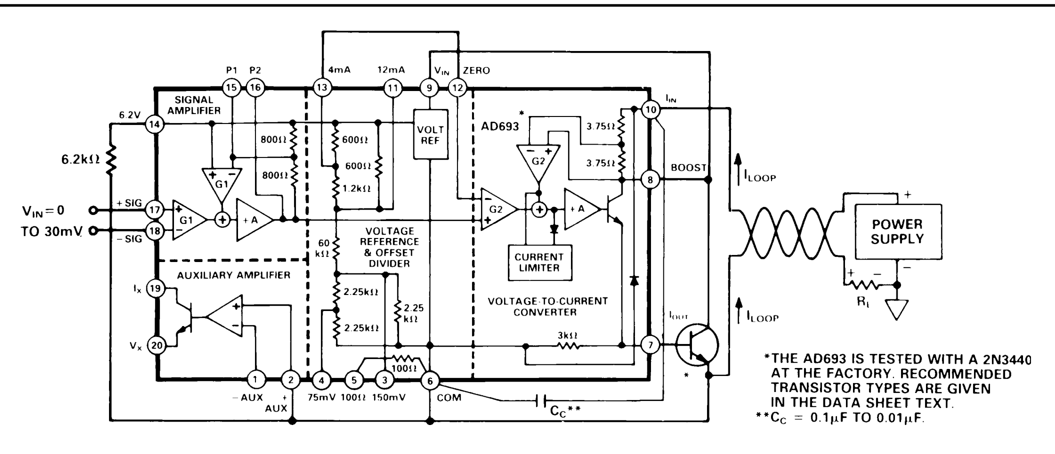


Figure 11. Using an External Pass Transistor to Minimize Self-Heating Errors

of adjustment of the output current from nominal. Substitute this value in the appropriate formula below for adjustment at the 4 mA tap.

$R_{Z1} = (1.6\ V/I_A) - 400\ \Omega$ and

$R_{Z2} = R_{Z1} \times 3.1\ V/(15\ mV + I_A \times 3.75\ \Omega)$

Use a similar connection with the following resistances for adjustments at the 12 mA tap.

$R_{Z1} = (4.8\ V/I_A) - 400\ \Omega$ and

$R_{Z2} = R_{Z1} \times 3.1\ V/(45\ mV + I_A \times 3.75\ \Omega)$

These formulae take into account the ±10% tolerance of tap resistance and insure a minimum adjustment range of I_A. For example, choosing I_A = 200 µA will give a zero adjustment range of ±1% of the 20 mA full-scale output. At the 4 mA tap the maximum value of:

R_{Z1} = 1.6 V/200 µA – 400 Ω = 7.6 kΩ and

R_{Z2} = 7.6 kΩ × 3.1 V/(15 mV + 200 µA × 3.75 Ω) = 1.49 MΩ

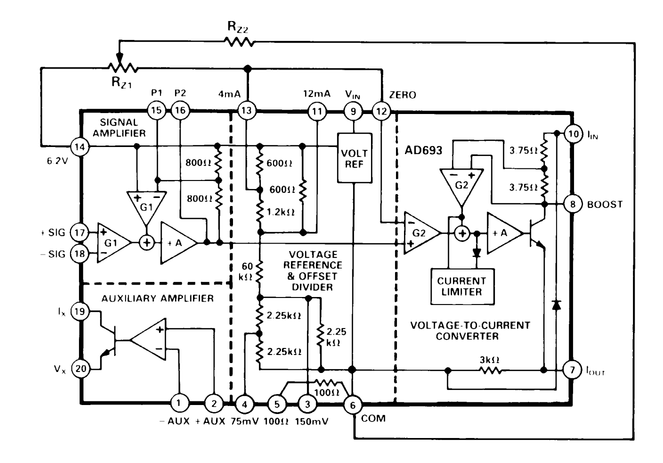


Figure 12. Optional 4 mA Zero Adjustment (12 mA Trim Available Also)

These can be rounded down to more convenient values of 7.5 kΩ and 1.3 MΩ, which will result in an adjustment range comfortably greater than ±200 µA.

ADJUSTING INPUT SPAN

Input Span is adjusted by changing the gain of the Signal Amplifier. This amplifier provides a 0-to-60 mV signal to the V/I section to produce the 4-to-20 mA output span (or a 0-to-75 mV signal in the 0-to-20 mA mode). The gain of this amplifier is trimmed to 2.00 so that an input signal ranging from 0-to-30 mV will drive the V/I section to produce 4-to -20 mA. Joining P1 and P2 (Pins 15 and 16) will reduce the Signal Amplifier gain to one, thereby requiring a 60 mV signal to drive the V/I to a full 20 mA span.

To produce spans less than 30 mV, an external resistor, R_{S1}, can be connected between P1 and 6.2 V. The nominal value is given by:

$$R_{S1} = \frac{400\ \Omega}{\frac{30\ mV}{S} - 1}$$

where S is the desired span. For example, to change the span to 6 mV a value of:

$$R_{S1} = \frac{400\ \Omega}{\frac{30\ mV}{6\ mV} - 1} = 100\ \Omega$$

is required. Since the internal, 800 Ω gain setting resistors exhibit an absolute tolerance of 10%, R_{S1} should be provided with up to ±10% range of adjustment if the span must be well controlled.

For spans between 30 mV and 60 mV a resistor R_{S2} should be connected between P1 and P2. The nominal value is given by:

$$R_{S2} = \frac{400\ \Omega \left(1 - \frac{60\ mV}{S}\right)}{\frac{30\ mV}{S} - 1}$$

For example, to change the span to 40 mV, a value of:

$$R_{S2} = \frac{400\ \Omega \left(1 - \frac{60\ mV}{40\ mV}\right)}{\frac{30\ mV}{40\ mV} - 1} = 800\ \Omega$$

is required. Remember that this is a nominal value and may require adjustment up to ±10%. In many applications the span must be adjusted to accommodate *individual* variations in the sensor as well as the AD693. The span changing resistor should, therefore, include enough adjustment range to handle both the sensor uncertainty and the absolute resistance tolerance of P1 and P2. Note that the temperature coefficient of the internal resistors is nominally –17 ppm/°C, and that the external resistors should be comparably stable to insure good temperature performance.

An alternative arrangement, allowing wide range span adjustment between two set ranges, is shown in Figure 13. R_{S1} and R_{S2} are calculated to be 90% of the values determined from the previous formulae. The smallest value is then placed in series with the wiper of the 1.5 kΩ potentiometer shown in the figure. For example, to adjust the span between 25 mV and 40 mV, R_{S1} and R_{S2} are calculated to be 2000 Ω and 800 Ω, respectively. The smaller value, 800 Ω, is then reduced by 10% to cover the possible ranges of resistance in the AD693 and that value is put in place.

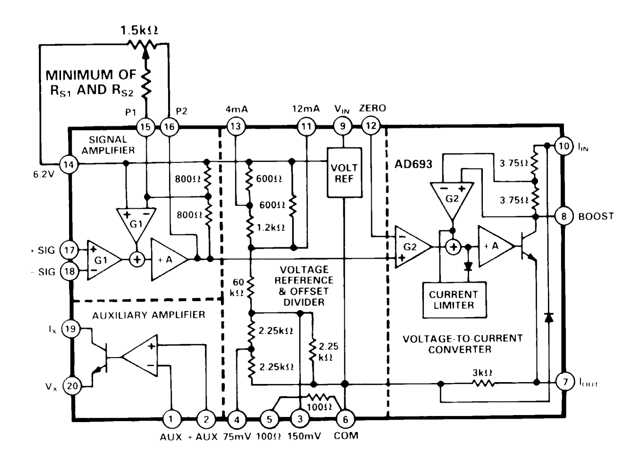


Figure 13. Wide Range Span Adjustment

A number of other arrangements can be used to set the span as long as they are compatible with the pretrimmed noninverting gain of two. The span adjustment can even include thermistors or other sensitive elements to compensate the span of a sensor.

In devising your own adjustment scheme, remember that you should adjust the gain such that the desired span voltage at the Signal Amplifier input translates to 60 mV at the output. Note also that the full differential voltage applied to the V/I converter is 75 mV; in the 4-20 mA mode, –15 mV is applied to the inverting input (zero pin) by the Divider Network and +60 mV is applied to the noninverting input by the Signal Amplifier. In the 0–20 mA mode, the total 75 mV must be applied by the Signal Amplifier. As a result, the total span voltage will be 25% larger than that calculated for a 4-20 mA output.

Finally, the external resistance from P2 to 6.2 V should not be made less than 1 kΩ unless the voltage reference is loaded to at least 1.0 mA. (A simple load resistor can be used to meet this requirement if a low value potentiometer is desired.) In no case should the resistance from P2 to 6.2 V be less than 200 Ω.

Input Spans Between 60 mV and 100 mV

Input spans of up to 100 mV can be obtained by adding an offset proportional to the output signal into the zero pin of the V/I converter. This can be accomplished with two resistors and adjusted via the optional trim scheme shown in Figure 14. The resistor divider formed by R_{E1} and R_{E2} from the output of the Signal Amplifier modifies the differential input voltage range applied to the V/I converter.

In order to determine the fixed resistor values, R_{E1} and R_{E2}, first measure the source resistance (R_D) of the internal divider network. This can be accomplished (power supply disconnected) by measuring the resistance between the 4 mA of offset (Pin 13) and common (Pin 6) with the 6.2 V reference (Pin 14) connected to common. The measured value, R_D, is then used to calculate R_{E1} and R_{E2} via the following formula:

$$R_{E2} = R_D\left(\frac{S}{S - 60\ mV} - 1.0024\right)$$

and $R_{E1} = 412\ R_{E2}$

Figure 14 shows a scheme for adjusting the modified span and 4 mA offset via R_{E3} and R_{E4}. The trim procedure is to first connect both signal inputs to the 6.2 V Reference, set R_{E4} to zero and then adjust R_{E3} so that 4 mA flows in the current loop. This in effect, creates a divider with the same ratio as the internal divider that sets the 4 mA zero level (–15 mV with respect to 6.2 V). As long as the input signal remains zero the voltage at Pin 12, the zero adjust, will remain at –15 mV with respect to 6.2 V.

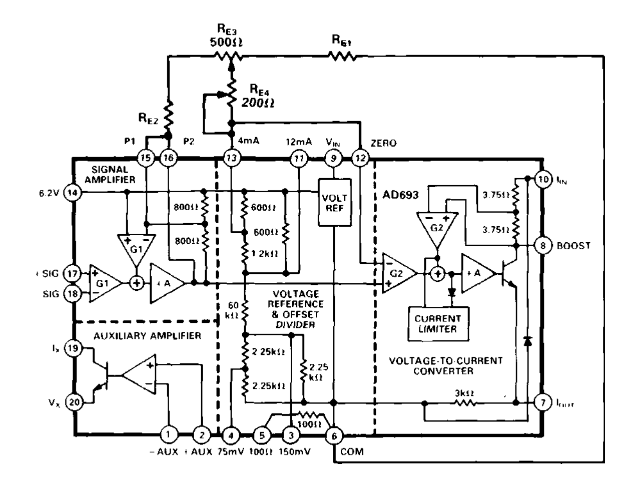


Figure 14. Adjusting for Spans between 60 mV and 100 mV (R_{E1} and R_{E2}) with Fine-Scale Adjust (R_{E3} and R_{E4})

After adjusting R_{E3} place the desired full scale (S) across the signal inputs and adjust R_{E4} so that 20 mA flows in the current loop. An attenuated portion of the input signal is now added into the V/I zero to maintain the 75 mV maximum differential. If there is some small offset at the input to the Signal Amplifier, it may be necessary to repeat the two adjustments.

LOCAL-POWERED OPERATION FOR 0–20 mA OUTPUT

The AD693 is designed for local-powered, three-wire systems as well as two-wire loops. All its usual ranges are available in three-wire operation, and in addition, the 0–20 mA range can be used. The 0-20 mA convention offers slightly more resolution and may simplify the loop receiver, two reasons why it is sometimes preferred.

The arrangement, illustrated in Figure 15, results in a 0–20 mA transmitter where the precalibrated span is 37.5 mV. Connecting P1 to P2 will double the span to 75 mV. Sensor input and excitation is unchanged from the two-wire mode except for the 25% increase in span. Many sensors are ratiometric so that an increase in excitation can be used instead of a span adjustment.

In the local-powered mode, increases in excitation are made easier. Voltage compliance at the I_{IN} terminal is also improved; the loop voltage may be permitted to fall to 6 volts at the AD693, easing the trade-off between loop voltage and loop resistance. Note that the load resistor, R_L, should meter the current into Pin 10, I_{IN}, so as not to confuse the loop current with the local power supply current.

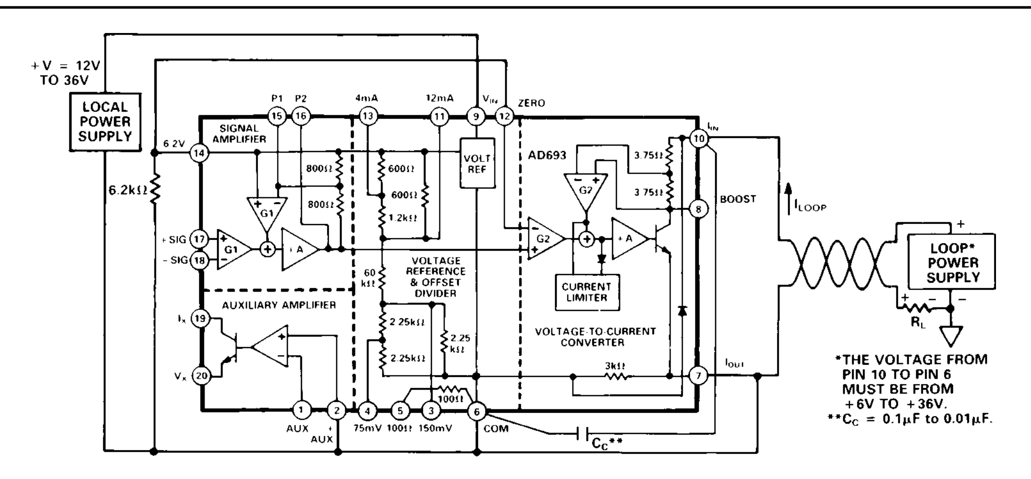


Figure 15. Local Powered Operation with 0–20 mA Output

OPTIONAL INPUT FILTERING

Input filtering is recommended for all applications of the AD693 due to its low input signal range. An RC filter network at each input of the signal amplifier is sufficient, as shown in Figure 16. In the case of a resistive signal source it may be necessary only to add the capacitors, as shown in Figure 18. The capacitors should be placed as close to the AD693 as possible. The value of the filter resistors should be kept low to minimize errors due to input bias current. Choose the 3 dB point of the filter high enough so as not to compromise the bandwidth of the desired signal. The RC time constant of the filter should be matched to preserve the ac common-mode rejection.

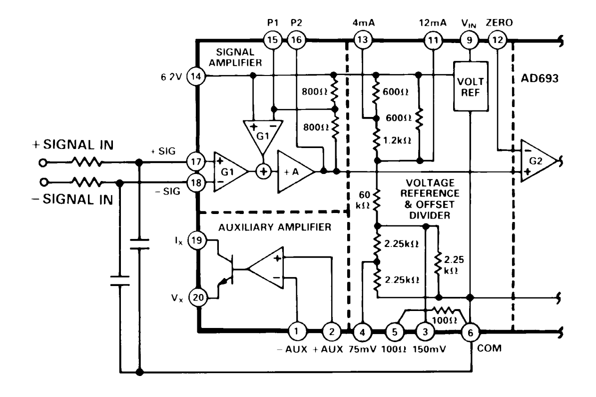


Figure 16. Optional Input Filtering

INTERFACING PLATINUM RTDS

The AD693 has been specially configured to accept inputs from 100 Ω Platinum RTDs (Resistance Temperature Detectors). Referring to Figure 17, the RTD and the temperature stable 100 Ω resistor form a feedback network around the Auxiliary Amplifier resulting in a noninverting gain of $(1 + R_T/100\ \Omega)$, where R_T is the temperature dependent resistance of the RTD. The noninverting input of the Auxiliary Amplifier (Pin 2) is then driven by the 75 mV signal from the Voltage Divider (Pin 4). When the RTD is at 0, its 100 Ω resistance results in an amplifier gain of +2 causing V_X to be 150 mV. The Signal Amplifier compares this voltage to the 150 mV output (Pin 3) so that zero differential signal results. As the temperature (and therefore, the resistance) of the RTD increases, V_X will likewise increase according to the gain relationship. The difference between this voltage and the zero degree value of 150 mV drives the Signal Amp to modulate the loop current. The AD693 is precalibrated such that the full 4-20mA output span corresponds to a 0 to 104°C range in the RTD. (This assumes the European Standard of $\alpha = 0.00385$.) A total of 6 precalibrated ranges for three-wire (or two-wire) RTDs are available using only the pin strapping options as shown in Table I.

A variety of other temperature ranges can be realized by using different application voltages. For example, loading the Voltage Divider with a 1.5 kΩ resistor from Pin 3 to Pin 6 (common) will approximately halve the original application voltages and allow for a doubling of the range of resistance (and therefore, temperature) required to fill the two standard spans. Likewise,

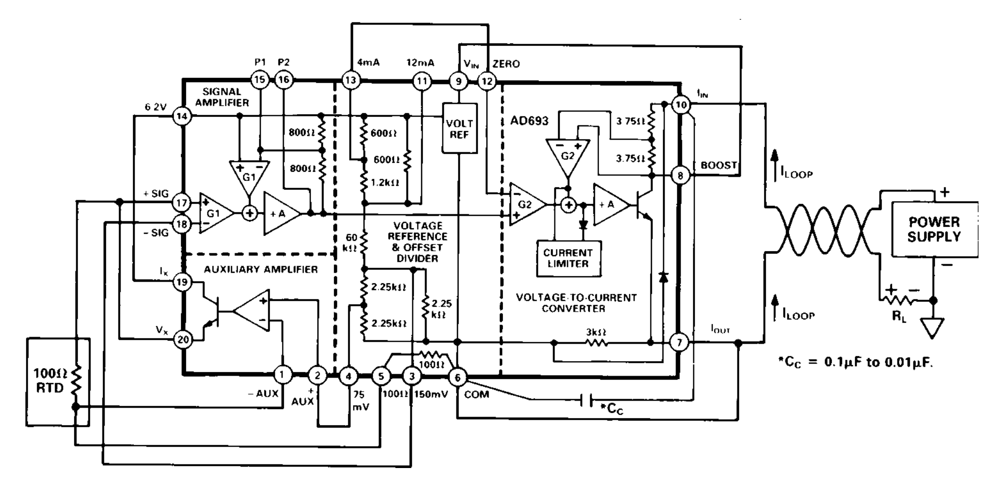


Figure 17. 0-to-104°C Direct Three-Wire 100 Ω RTD Interface, 4-20mA Output

Table I. Precalibrated Temperature Range Options Using a European Standard 100 Ω RTD and the AD693

Temperature Range	Pin Connections
0 to + 104°C	12 to 13
0 to +211°C	12 to 13, and 15 to 16
+25°C to +130°C	12 to 14
+51°C to +266°C	12 to 14, and 15 to 16
–50°C to +51°C	12 to 11
–100°C to +104°C	12 to 11 and 15 to 16

increasing the application voltages by adding resistance between Pins 14 and 3 will decrease the temperature span.

An external voltage divider may also be used in conjunction with the circuit shown to produce any range of temperature spans as well as providing zero output (4 mA) for a non 0 temperature input. For example, measuring V_X with respect to a voltage 2.385 times the excitation (rather than 2 times) will result in zero input to the Signal Amplifier when the RTD is at 100°C (or 138.5 Ω).

As suggested in Table I, the temperature span may also be adjusted by changing the voltage span of the Signal Amplifier. Changing the gain from 2 to 4, for example, will halve the temperature span to about 52°C on the 4-20mA output configuration. (See section "Adjusting Input Span.")

The configuration for a three-wire RTD shown in Figure 17 can accommodate two-wire sensors by simply joining Pins 1 and 5 of the AD693.

INTERFACING LOAD CELLS AND METAL FOIL STRAIN GAGES

The availability of the on-chip Voltage Reference, Auxiliary Amplifier and 3 mA of excitation current make it easy to adapt the AD693 to a variety of load cells and strain gages.

The circuit shown in Figure 18 illustrates a generalized approach in which the full flexibility of the AD693 is required to interface to a low resistance bridge. For a high impedance transducer the bridge can be directly powered from the 6.2 V Reference.

Component values in this example have been selected to match the popular standard of 2 mV/V sensitivity and 350 Ω bridge resistance. Load cells are generally made for either tension and compression, or compression only; use of the 12 mA zero tap allows for operation in the tension and compression mode. An optional zero adjustment is provided with values selected for ±2% FS adjustment range.

Because of the low resistance of most foil bridges, the excitation voltage must be low so as not to exceed the available 4 mA zero current. About 1 V is derived from the 6.2 V Reference and an external voltage divider; the Aux-Amp is then used as a follower to make a stiff drive for the bridge. Similar applications with higher resistance sensors can use proportionally higher voltage.

Finally, to accommodate the 2 mV/V sensitivity of the bridge, the full-scale span of the Signal Amplifier must be reduced. Using the load cell in both tension and compression with 1 V of excitation, therefore, dictates that the span be adjusted to 4 mV. By substituting in the expression, $R_{S1} = 400\ \Omega/[(30\ mV/S) - 1]$, the nominal resistance required to achieve this span is found to be 61.54 Ω. Calculate the minimum resistance required by subtracting 10% from 61.54 Ω to allow for the internal resistor tolerance of the AD693, leaving 55.38 Ω (See "Adjusting Input Span.") The standard value of 54.9 Ω is used with a 20 Ω potentiometer for full-scale adjustment.

If a load cell with a precalibrated sensitivity constant is to be used, the resultant full-scale span applied to the Signal Amplifier is found by multiplying that sensitivity by the excitation voltage. (In Figure 18, the excitation voltage is actually (10 kΩ/62.3 kΩ) (6.2 V) = 0.995 V).

THERMOCOUPLE MEASUREMENTS

The AD693 can be used with several types of thermocouple inputs to provide a 4-20 mA current loop output corresponding to a variety of measurement temperature ranges. Cold junction compensation (CJC) can be implemented using an AD592 or AD590 and a few external resistors as shown in Figure 19.

From Table II simply choose the type of thermocouple and the appropriate average reference junction temperature to select values for R_{COMP} and R_Z. The CJC voltage is developed across R_{COMP} as a result of the AD592 1 μA/K output and is added to the thermocouple loop voltage. The 50 Ω potentiometer is biased by R_Z to provide the correct zero adjustment range appropriate for the divider and also translates the Kelvin scale of the AD592 to °Celsius. To calibrate the circuit, put the thermocouple in an ice bath (or use a thermocouple simulator set to 0) and adjust the potentiometer for a 4 mA loop current.

The span of the circuit in °C is determined by matching the signal amplifier input voltage range to its temperature equivalent

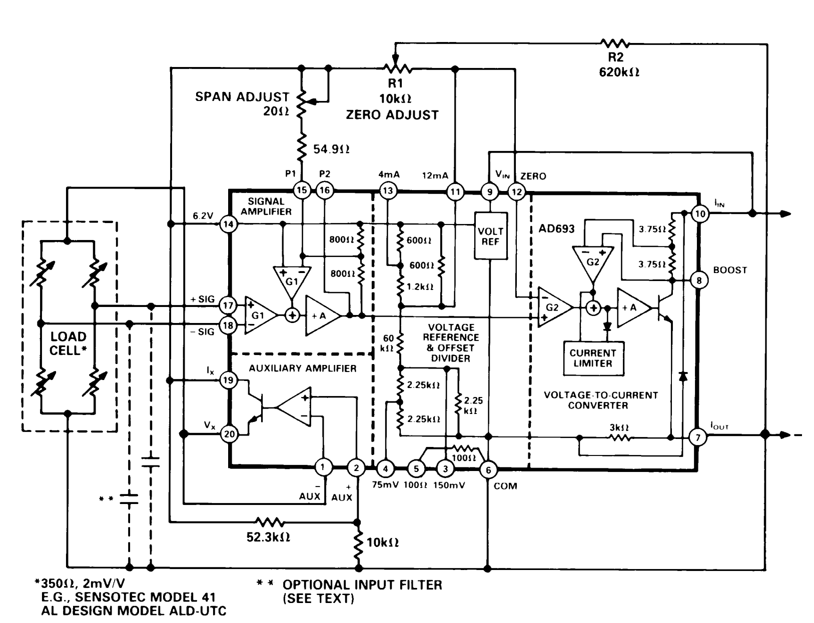


Figure 18. Utilizing the Auxiliary Amplifier to Drive a Load Cell, 12 mA ± 8 mA Output

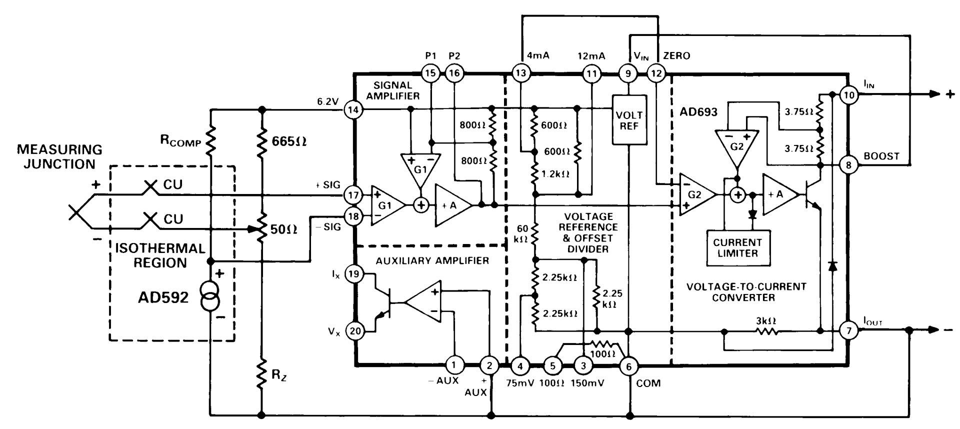


Figure 19. Thermocouple Inputs with Cold Junction Compensation

Table II. Thermocouple Application—Cold Junction Compensation

POLARITY	MATERIAL	TYPE	AMBIENT TEMP	RCOMP	RZ	30 mV TEMP RANGE	60 mV TEMP RANGE
+	IRON	J	25°	51.7 Ω	301K	546°C	1035°C
–	CONSTANTAN		75°	53.6 Ω	294K		
+	NICKEL-CHROME		25°	40.2 Ω	392K	721°C	—
–	NICKEL-ALUMINUM	K	75°	42.2 Ω	374K		
+	NICKEL-CHROME	E	25°	60.4 Ω	261K	413°C	787°C
–	COPPER-NICKEL		75°	64.9 Ω	243K		
+	COPPER	T	25°	40.2 Ω	392K	USE WITH GAIN >2	
–	COPPER-NICKEL		75°	45.3 Ω	340K		

via a set of thermocouple tables referenced to °C. For example, the output of a properly referenced type J thermocouple is 60 mV when the hot junction is at 1035°C. Table II lists the maximum measurement temperature for several thermocouple types using the preadjusted 30 mV and 60 mV input ranges.

More convenient temperature ranges can be selected by determining the full-scale input voltages via standard thermocouple tables and adjusting the AD693 span. For example, suppose only a 300°C span is to be measured with a type K thermocouple. From a standard table, the thermocouple output is 12.207 mV; since 60 mV at the signal amplifier corresponds to a 16 mA span at the output a gain of 5, or more precisely 60 mV/12.207 mV = 4.915 will be needed. Using a 12.207 mV span in the gain resistor formula given in "Adjusting Input Span" yields a value of about 270 Ω as the minimum from P1 to 6.2 V. Adding a 50 Ω potentiometer will allow ample adjustment range.

With the connection illustrated, the AD693 will give a full-scale indication with an open thermocouple.

ERROR BUDGET ANALYSIS

Loop-Powered Operation specifications refer to parameters tested with the AD693 operating as a loop-powered transmitter. The specifications are valid for the preset spans of 30 mV, 60 mV and those spans in between. The section, "Components of Error," refers to parameters tested on the individual functional blocks, (Signal Amplifier, V/I Converter, Voltage Reference, and Auxiliary Amplifier). These can be used to get an indication of device performance when the AD693 is used in local power mode or when it is adjusted to spans of less than 30 mV.

Table III lists the expressions required to calculate the total error. The AD693 is tested with a 250 Ω load, a 24 V loop supply

Table III. RTI Contributions to Span and Offset Error

RTI Contributions to Offset Error

	Error Source	Expression for RTI Error at Zero
I_{ZE}	Zero Current Error	I_{ZE}/X_S
PSRR	Power Supply Rejection Ratio	$(\lvert V_{LOOP} - 24\text{ V}\rvert + [\lvert R_L - 250\ \Omega\rvert \times I_Z]) \times \text{PSRR}$
CMRR	Common-Mode Rejection Ratio	$\lvert V_{CM} - 3.1\text{ V}\rvert \times \text{CMRR}$
IOS	Input Offset Current	$R_S \times \text{IOS}$

RTI Contributions to Span Error

	Error Source	Expression for RTI Error at Full Scale
X_{SE}	Transconductance Error	$V_{SPAN} \times X_{SE}$
X_{PSRR}	Transconductance PSRR[1]	$\lvert R_L - 250\ \Omega\rvert \times I_S \times \text{PSRR}$
X_{CMRR}	Transconductance CMRR	$\lvert V_{CM} - 3.1\text{ V}\rvert \times V_{SPAN} \times X_{CMRR}$
X_{NL}	Nonlinearity	$V_{SPAN} \times X_{NL}$
I_{DIFF}	Differential Input Current[2]	$RS \times I_{DIFF}$

Abbreviations

I_Z	Zero Current (usually 4 mA)
I_S	Output span (usually 16 mA)
R_S	Input source impedance
R_L	Load resistance
V_{LOOP}	Loop supply voltage
V_{CM}	Input common-mode voltage
V_{SPAN}	Input span
X_S	Nominal transconductance in A/V

[1]The 4–20 mA signal, flowing through the metering resistor, modulates the power supplyvoltage seen by the AD693. The change in voltage causes a power supply rejection error that varies with the output current, thus it appears as a span error.

[2]The input bias current of the inverting input increases with input signal voltage. The differential input current, I_{DIFF}, equals the inverting input current minus the noninverting input current; see Figure 2. I_{DIFF}, flowing into an input source impedance, will cause an input voltage error that varies with signal. If the change in differential input current with input signal is approximated as a linear function, then any error due to source impedance may be approximated as a span error. To calculate I_{DIFF}, refer to Figure 2 and find the value for I_{DIFF}/ + In corresponding to the full-scale input voltage for your application. Multiply by + In max to get I_{DIFF}. Multiply I_{DIFF} by the source impedance to get the input voltage error at full scale.

and an input common-mode voltage of 3.1 V. The expressions below calculate errors due to deviations from these nominal conditions.

The total error at zero consists only of offset errors. The total error at full scale consists of the offset errors plus the span errors. Adding the above errors in this manner may result in an error as large as 0.8% of full scale, however, as a rule, the AD693 performs better as the span and offset errors do not tend to add worst case. The specification "Total Unadjusted Error," (TUE), reflects this and gives the maximum error as a % of full scale for any point in the transfer function when the device is operated in one of its preset spans, with no external trims. The TUE is less than the error you would get by adding the span and offset errors worst case.

Thus, an alternative way of calculating the total error is to start with the TUE and add to it those errors that result from operation of the AD693 with a load resistance, loop supply voltage, or common-mode input voltage different than specified. (See Example 1 below.)

ERROR BUDGET FOR SPANS LESS THAN 30 mV

An accommodation must be made to include the input voltage offset of the signal amplifier when the span is adjusted to less than 30 mV. The TUE and the Zero Current Error include the input offset voltage contribution of the signal amplifier in a gain of 2. As the input offset voltage is multiplied by the gain of the signal amplifier, one must include the additional error when the signal amplifier is set to gains greater than 2.

For example, the 300K span thermocouple application discussed previously requires a 12.207 mV input span; the signal amplifier must be adjusted to a gain of approximately 5. The loop transconductance is now 1.333 A/V, (5 × 0.2666 A/V). Calculate the total error by substituting the new values for the transconductance and span into the equations in Table III as was done in Example I. The error contribution due to V_{OS} is 5 × V_{OS}, however, since 2 × V_{OS} is already included in the TUE and the Zero Current Error it is necessary to add an error of only (5 – 2) × V_{OS} to the error budget. Note that span error may by reduced to zero with the span trim, leaving only the offset and nonlinearity of the AD693.

EXAMPLE I

The AD693 is configured as a 4-20mA loop powered transmitter with a 60 mV FS input. The inputs are driven by a differential voltage at 2 V common mode with a 300 Ω balanced source resistance. A 24 V loop supply is used with a 500 Ω metering resistance. (See Table IV below.)

Trimming the offset and span for your application will remove all span and offset errors except the nonlinearity of the AD693.

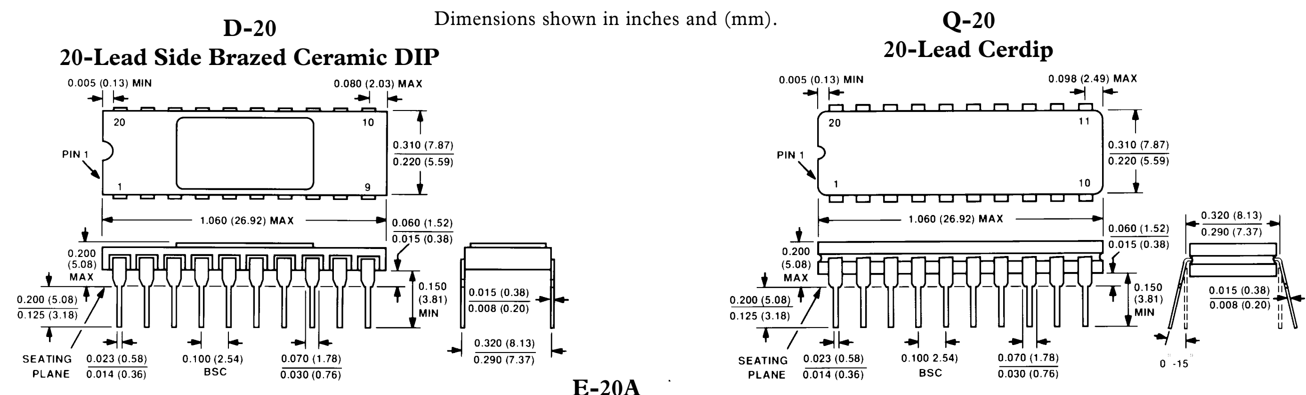
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Table IV. Example 1

OFFSET ERRORS		
I_Z	Already included in the TUE spec .	0.0 µV
PSRR	PSRR = 5.6 µV/V; (|24 V – 24 V| + [| 500 Ω – 250 Ω × 4 mA]) × 5.6 µV/V =	5.6 µV
	V_{LOOP} = 24 V	
	R_L = 500 Ω I_Z = 4 mA	
CMRR	CMRR = 30 µV/V; |2 V –3.1 V| × 30 µV/V =	33.0 µV
	V_{CM} = 2 V	
IOS	IOS = 3 nA, R_S = 300 Ω; 300 Ω × 3 nA =	0.9 µV
Total Additional Error at 4 mA		**39.5 µV**
As % of full scale; (39.5 µV × 0.2666 A/V)/20 mA × 100% =		0.053 % of FS
SPAN ERRORS		
X_{SE}	Already included in the TUE spec	0.0 µV
X_{PSRR}	PSRR = 5.6 µV/V; (|500 Ω – 250 Ω| × 16 mA) × 5.6 µV/V =	22.4 µV
	R_L = 500 Ω, I_S = 16 mA	
X_{CMRR}	X_{CMRR} = 0.06%/V; |2 V – 3. 1 V| × 60 mV × 0.06%/V =	39.6 µV
	V_{CM} = 2 V, V_{SPAN} = 60 mV	
I_{DIFF}	V_{SPAN} = +60 mV; 300 Ω × 2 × 20 nA	12.0 µV
	I_{DIFF}/ + In = 2	
	from Figure 2)	
X_{NL}	Already included in the TUE	0.0 µV
Total Additional Span Error at Full Scale		**74.0 µV**
Total Additional Error at Full Scale; ϵ_{OFFSET} + ϵ_{SPAN} = 39.5 µV + 74.0 µV =		113.5 µV
As % of Full Scale; (113.5 µV × 0.2666A V)/20 mA × 100% =		0.151% of FS
New Total Unadjusted Error @ FS; ϵ_{TUE} + $\epsilon_{ADDITIONAL}$ = 0.5% +0.151% =		**0.651% of FS**

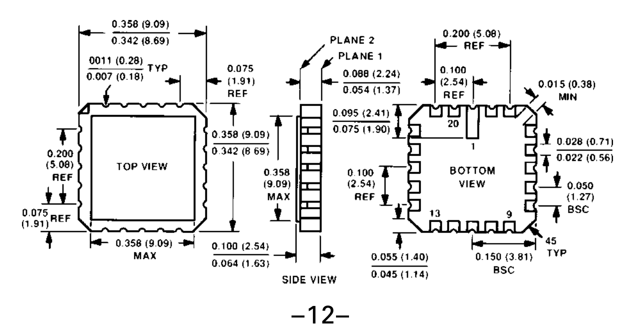
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



E-20A

20-Terminal Leadless Chip Carrier



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